

Notice of References Cited	Application/Control No. 10/697,406	Applicant(s)/Patent Under Reexamination GUENTHNER ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Beraudo et al., "Timing Optimization of FPGA Placement by Logic Replication," ACM 2003, June 3-6, 2003, pages 196-201.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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